REMARKS/ARGUMENTS

Claims 17-20 and 22-30 are currently pending in the above-identified application, with claim 17 being the sole independent claim. Claim 21 has been canceled. Claims 17, 19 and 22-29 have been amended.

The Office Action contains an objection to the drawings under 37 C.F.R. §1.83(a) for failing to show field isolation areas 100 (page 2, section 3). This objection is not understood. Field isolation areas 100 are shown at the left and right ends of Fig. 1. Accordingly, the objection to the drawings should be withdrawn.

The Office Action contains additional objections to the drawings under 37 C.F.R. §1.83(a) regarding the use of reference characters 128 and 129 (page 3, section 4) and reference sign 114 (page 3, section 5). In response, the specification has been amended so that no corrections to the drawings are needed. Accordingly, the objection to the drawings should be withdrawn.

Claims 17-30 have been rejected under 35 U.S.C. §112(2) for being indefinite (page 3, section 10 through page 5, section 24). In response, claims 17 and 23-29 have been amended. However, the rejection to claim 23 regarding the antecedent basis of said conductive plug (page 4, section 13) is not understood. Line 2 of claim 23 recites "a conductive plug", while line 3 of claim 23 recites "said conductive plug". Thus, proper antecedent basis for the conductive plug is established. Accordingly, the 112(2) rejection should be withdrawn.

Claims 17 and 19 have been amended to replace "fast ion conductor" with material having a "changeable resistance". Support for this amendment can be found at least within paragraphs 16 and 17 of the specification.

Claims 17-20 and 23-38 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Katori in view of Ovshinsky. Claim 17 has been amended to incorporate the subject matter of claim 21, which was indicated as allowable (Office Action, page 8,

section 39). Thus, the rejection of claim 17 as well as all claims dependent therefrom should be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By _____

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Version With Markings to Show Changes Made

IN THE TITLE:

Please amend the title as follows.

[APPARATUS AND] METHOD [FOR] OF FABRICATING DUAL PCRAM CELLS [CELL] SHARING A COMMON ELECTRODE [PCRAM MEMORY DEVICE]

IN THE SPECIFICATION:

Please amend paragraph 10 as follows.

Another insulating layer 112 of, for example, silicon nitride is then formed over the Fig. 3 structure, and is patterned to form openings over the chalcogenide glass areas. An Ag/W/Ag conductive stack 110, for example, is then formed in the openings, as shown in Fig. 4. This conductive stack combination serves as [a] an anode 110 for the lower memory cell 118 formed by the cathode 104, chalcogenide glass 105, and anode 110, and serves as the anode for an upper memory cell, the formation of which is described below. The Ag/W/Ag stack [114] 110 may be fabricated across a memory cell array. Electrical connections to the stacks [114] 110 can be made at the periphery contact holes of a memory cell array.

Please amend paragraph 11 as follows.

In the next stage of fabrication, show in Fig. 5, another insulating layer 124, for example, silicon nitride, is deposited and patterned to form holes 126 over the anodes 110. A silver and chalcogenide glass layer [128] 129 is then deposited with the holes 126 and planarized. As with layer 105, the chalcogenide glass may be formed as an Ag/Ge_3Se_7

material, or other chalcogenized glass compositions, which are capable of focusing a conductive path in the presence of an applied voltage or other glass compositions which can be used to write or read data may also be used. As also shown in Fig. 6, another insulating layer 131 is deposited and patterned to form holes and a conductor 130, such as tungsten, is then deposited in the holes in contact with chalcogenide glass layer [128] 129. A layer of tungsten 130b is also deposited in a hole provided in layer 131 over polysilicon plug 29b. The tungsten electrodes 130a serve as cathodes 132 for the upper chalcogenide glass memory cell 120 formed by common anode 110 and chalcogenide layer 129. Unlike cathodes 104, cathodes 132 are formed solely from tungsten. Additional fabrication steps can now be used to connect cathodes 132 to respective access transistors similar to transistors 15a, 15b and formed elsewhere in the memory cell array.

Please amend paragraph 17 as follows.

Although Fig. 7 shows access transistor 120_{AT} connecting the upper memory cell 120 to a column line B, separate from column line A, since the memory cells 118, 120 are never accessed at the same time, access transistors can also be configured to couple the upper memory cell 120 to column line A. The use of a separate column line B for the upper memory cell [128] 120, however, would enable both cells to be accessed at the same time to simultaneously store and retrieve two bits of data. In such a case the grid decoder can be omitted.

IN THE CLAIMS:

Please amend the claims as follows.

17. (Amended) A method of fabricating a memory device comprising:

forming a first memory cell to include a chalcogenide glass material [containing a fast ion conductor] having a changeable resistance and cathode and anode electrodes spaced apart and in contact with said [fast ion conductor] chalcogenide glass material;

forming a second memory cell to include a chalcogenide glass material [containing a fast ion conductor] having a changeable resistance and cathode and anode electrodes spaced apart and in contact with said [fast ion conductor] chalcogenide glass material;

forming a common anode for both of said first and second memory cells, wherein said common anode comprises a middle conductive layer and a layer of silver on opposite sides of said middle conductive layer.

19. A method as in claim 17 further comprising:

forming each of said first and second memory cells of a layered structure which includes a cathode layer, a [fast ion conductor] chalcogenide glass material layer having a changeable resistance and a anode layer.

21. (cancel without disclaimer or prejudice)

22. A method as in claim [21] 17, wherein said middle conductive layer comprises tungsten.

23. (Amended) A method as in claim 18 further comprising:

forming said stacked first and second memory cells over a conductive plug such that [a] said cathode of said second memory cell is in electrically coupled with said conductive plug.

24. (Amended) A method as in claim 23 further comprising a column line conductor electrically coupled to a second active region of [said] a first access transistor.

25. (Amended) A method as in claim 23 [facing] further comprising forming a word line conductor which is electrically coupled to a gate of [said] a first access transistor.

26. (Amended) A method as in claim 23 further comprising forming a second access transistor and electrically coupling said second access transistor to said [upper] second memory cell.

27. (Amended) A method as in claim 26 wherein said [upper and lower] first and second memory cells are coupled to different column lines by said first and second access transistors.

28. (Amended) A method as in claim 17 wherein said [upper and lower] first and second memory cells are connected to the same column line by said first and second access transistors.

29. (Amended) A method as in claim 26 further comprising:

forming a circuit for operating said first and second access transistors separately to individually access each of said [upper and lower] first and second memory cells.